A 1GHz-band Low Distortion Up-converter with a Linear in dB Control VGA for Digital TV Tuner

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Abstract — **A new exponential controlled variable gain amplifier (VGA) and an up-mixer have been integrated in a single chip using 0.35μm CMOS process. The gain of the VGA is controlled analog-linear in dB by using proposed a multi-stage multi-control *R-r* ladder structure to cover the wide gain control range. Up-converter shows a low distorted IF output signal over the wide RF input signal range of 50MHz~810MHz for digital TV tuner. Measurements show that the gain control range of VGA is -48 ~ 0dB and the IIP3 of the overall up-converter is 27 ~ 1dBm, respectively. In addition, -3dB frequency is measured to 1GHz. The chip consumes 10mA with a single 3.3V power supply.**

I. INTRODUCTION

The block diagram of the digital TV tuner system is shown in Fig. 1. To meet our specifications for digital TV tuner, it is necessary for the up-converter to have the following properties: 1) A minimum gain control range of 40dB (-40 ~ 0dB) and a linear gain in dB as a function of control voltage; 2) Input signal dynamic range of 70dB (-80 ~ -10dBm) and a bandwidth of 1GHz; 3) All input and output impedance of 50Ω; 4) high IIP3 for large input power and low NF characteristics; 5) a single 3.3V power supply with a low current consumption [1].

A VGA is an essential component of a linear receiver to control the input-power level of mixer because the power level of the received signals varies with wide range. In a digital TV tuner, the maximum received signal level is very high compared to any other wireless system. Therefore, the VGA must have a wide gain control range and great linearity. In addition, the functional dependences of VGA gain on control voltage should be a constant loop gain of the automatic gain control (AGC), which leading to a uniform loop transient response and a guaranteed loop settling time. This is fulfilled in a VGA whose gain changes linearly in dB with control voltage.

Conventional VGAs utilize the degenerated source coupled amplifier for gain adjustment. Their disadvantage is the poor linearity under compressed gain conditions. This is because CMOS linearity degrades as *gm* or g_{ds} decreases. Moreover, CMOS is not a logarithmic device.

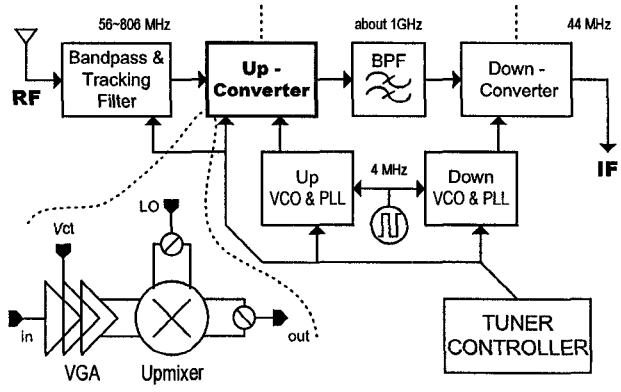

Fig. 1. Block diagram of the digital TV tuner system.

One possibility is to generate the required exponential characteristic using parasitic bipolar transistors. However, this leads to power consumption for exponential bleeding to bipolar devices as wide as dynamic range is.

These problems have been solved by the proposed new VGA configuration and gain control technique.

II. VGA : LINEAR IN dB CONTROL

The proposed VGA shown in Fig. 2 has a simple three-stage *R-r* ladder attenuation with dc level shift ('Δ' marked in Fig. 2) between stages, and has two control voltages. One is the external control voltage (*Vct*), and the other is the internally generated voltage (*Vc*) lower than *Vct* as much as δ (about Δ/2). The first stage is composed of R_1~R_2 and Mr_1~Mr_2. The second is M_3~M_4 and Mr_3~Mr_4. And the third is M_5~M_6 and Mr_5~Mr_6. The *gm* of M_3~M_6 is used as constant *R*, and the g_{ds} of Mr_1~Mr_6 operating in triode region is used as variable *r*.

In the first stage, especially, the rigid resistors R_1 and R_2 are used. This has two merits. One is that the resistors have no distortion, but CMOS suffers from its *gm* or g_{ds} distortion as input power increases (-10dBm in this spec.).

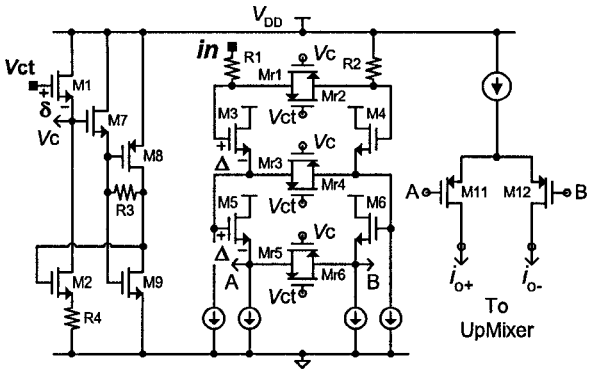

Fig. 2. New VGA configuration schematic.

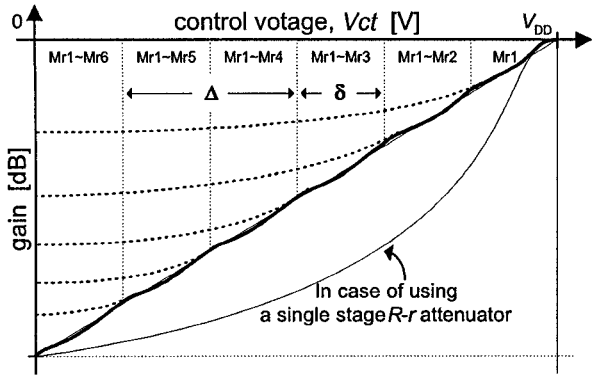

Fig. 3. Control principle of linear gain in dB.

And the other is that, due to no dc drop of R_1~R_2 and the δ (about CMOS threshold voltage) difference between *Vct* and *Vc*, it is possible to control the attenuation level with the full range of *Vct* from ground to V_{DD}. The resistance of R_1~R_2 is small as about 100Ω~200Ω to minimize noise contribution.

As is generally known, (1-x)/(1+x) is an approximation of the exponential function *exp*(-2x) [2]. And the *R-r* attenuation can be expressed as $1/(1+R*g_{ds})$. So, we can approximate the $1/(1+R*g_{ds})$ to $exp(-2R*g_{ds})$. It is well known that the g_{ds} is proportional to gate-source voltage ($g_{ds} \propto V_{gs}$) in triode region. Thus, we can control the gain of *R-r* attenuator in exponential function. However, a single stage of *R-r* attenuator only is not satisfactory to obtain an exponential function in the required dynamic range.

Therefore, we constitute a multi-stage multi-control *R-r* attenuator operating in exponential function. This is feasible owing to the dc level shift (Δ) between stages and the difference (δ) of the control voltages. As the control voltages (*Vct*, *Vc*) increase (or decrease), the linear transistors (Mr_1~Mr_6) are additively turn-off (or turn-on).

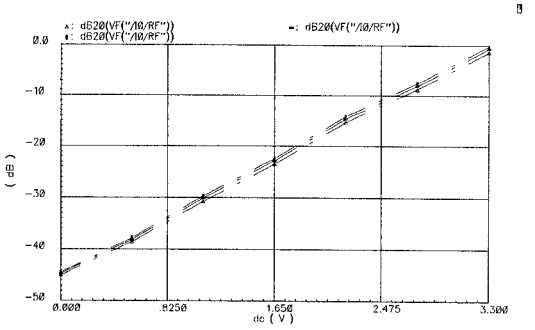

Fig. 4. Linear in dB control of the VGA.
(Top: 50MHz, Middle: 400MHz, Bottom: 800MHz)

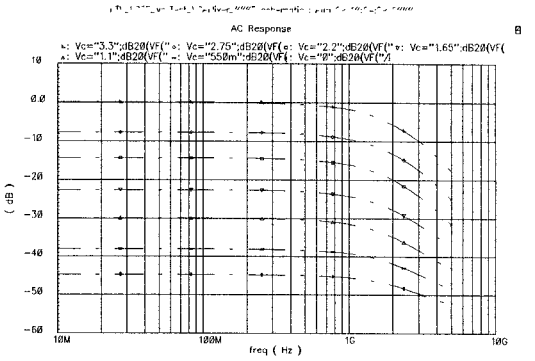

Fig. 5. Frequency response of the VGA. (f_{-3dB} is >1GHz)

Hence, it is possible that the proposed VGA's gain changes linearly in dB with the full range of control voltage. This operation is well shown in Fig. 3.

The VGA in Fig. 2 is simulated using CADENCE, and the waveforms are depicted in Fig. 4 and 5. Fig. 4 shows that the controlled gain waveforms irrespective to frequency variation are very linear in dB range. In addition, Fig. 5 shows that the bandwidth of the VGA core in Fig. 2 is over than 1GHz.

Compared with any other exponential gain control method, the proposed technique is based on the empirical as well as numerical method. In fact, the present sub-micron CMOS technology does not follow a general square law expression (practically, 1~2 square for V_{gs}). Despite of the varying rule, the proposed technique can be adopted after optimizing by simulations and measurements. For example, the *Vc* generation circuit in Fig. 2 has been designed after simulation results.

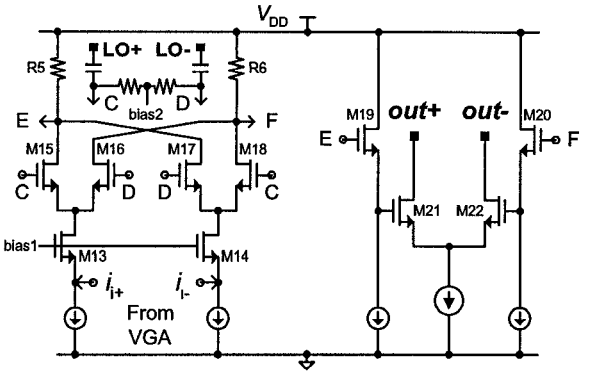

Fig. 6. Upmixer schematic.

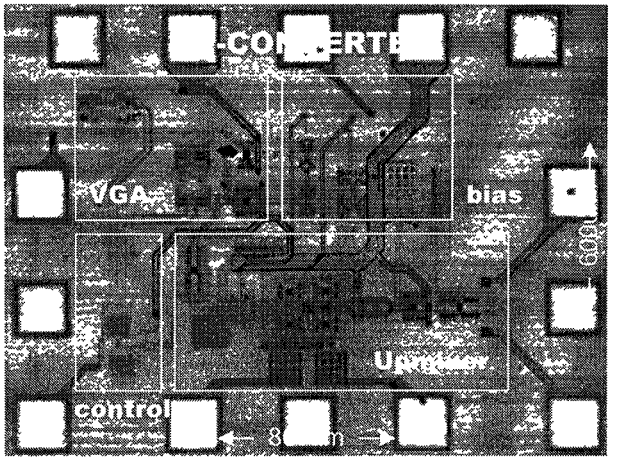

Fig. 7. Micrograph of up-converter chip.

III. UP MIXER

To perform the frequency translation from RF to the first IF, the circuit topology of a Gilbert cell four-quadrant multiplier is used in the designed double balanced up-conversion mixer as shown in Fig. 6. The RF transconductance stage of the upmixer consists of the PMOS differential pair M_{11} and M_{12} in Fig. 2. The upmixer employs a folded cascode connection composed of M_{11}~M_{14}, which has two main advantages. First, dc blocking capacitors are not required. Thus, the low RF frequency about 50MHz can be passed to the upmixer without degradation. Second, compared to the conventional Gilbert cell topology, the reverse isolation from upmixer to VGA due to the LO-RF feedthrough is improved. The up-converted signal goes out through the open drain transconductance differential amplifier with buffer stage, and drives external 50Ω load.

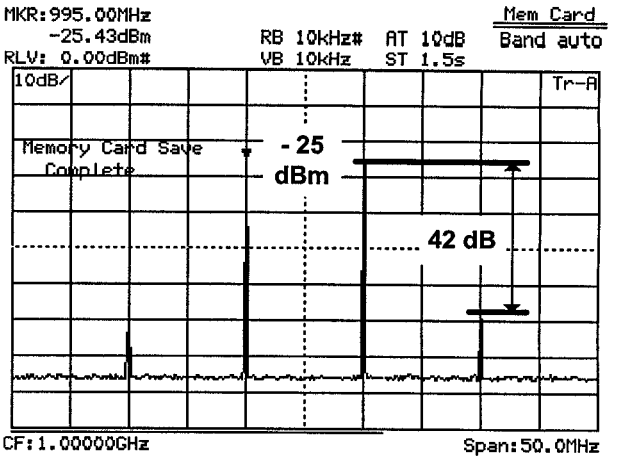

Fig. 8. Frequency spectrum of the up-converter output. Gain is 0dB (assume -5dBm loss) and IIP3 is 1dBm (RF= -20dBm at 395&405MHz, LO= 0dBm at 1400MHz)

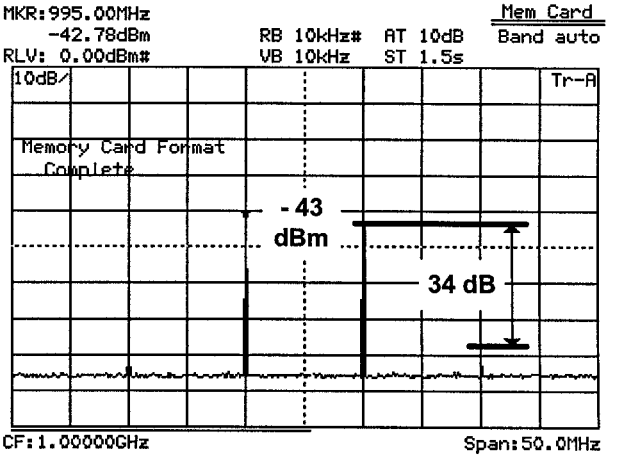

Fig. 9. Frequency spectrum of the up-converter output. Gain is -48dB (assume -5dBm loss) and IIP3 is 27dBm (RF= 10dBm at 395&405MHz, LO= 0dBm at 1400MHz)

IV. EXPERIMENTAL RESULTS

The up-converter, with the proposed gain control topology, has been designed with the RF device models developed in our lab, and fabricated in a standard 0.35μm CMOS technology. A die photograph is shown in Fig. 7. All transistors passing through differential signal have a common centroid layout to improve balancing. In measurements, two balun transformers are used for differential signal of LO input and the first IF output, and external networks are set to match all the input and output ports to 50Ω.

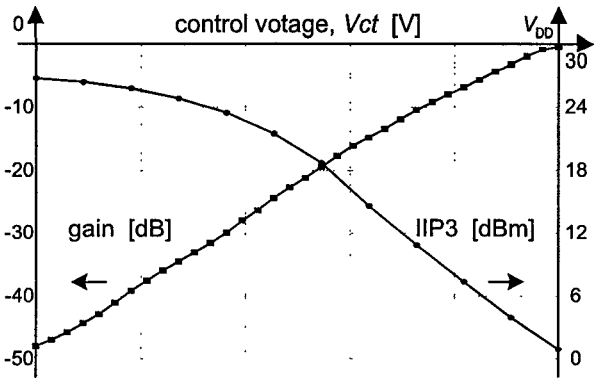

Fig. 10. Gain and IIP3 characteristic of the up-converter.

Fig. 8 and 9 show the measured frequency spectrum of the up-converter. The overall power loss in measurement setup is assumed as about 5dBm. This value is very reasonable considering the losses of balun transformers and cables. The measurements show that the gain control and intermodulation characteristics have the desired results. The gain control range is about 48dB (-48 ~ 0dB). The VGA is controlled with linear gain in dB scale in terms of the control voltage. Note also that the IIP3 is 27dBm at minimum gain and 1dBm at maximum gain. The gain control and intermodulation characteristics are depicted in Fig. 10. In addition, the measurements also show that the -3dB frequency of the up-converter is about 1GHz.

V. CONCLUSION

We propose the new exponential controlled variable gain amplifier (VGA) and an up-mixer have been integrated in a single chip using 0.35μm CMOS process. The gain of the VGA is controlled analog-linear in dB by using proposed a multi-stage multi-control *R-r* ladder structure to cover the wide gain control range. The up-converter shows a low distorted IF output signal over the wide RF input signal range of 50MHz~810MHz for digital TV tuner. Measurements show that the gain control range of VGA is -48 ~ 0dB and the IIP3 of the overall up-converter is 27 ~ 1dBm, respectively. In addition, -3dB frequency is measured to 1GHz. The chip consumes 10mA with a single 3.3V power supply.

The overall measured performances are summarized in table 1.

TABLE 1 : Summary of the up-converter performance

Technology: 0.35μm CMOS with 2-poly and 4 metal
Power Consumption: 10mA at 3.3V supply
Dynamic range: -48 ~ 0dB over 50MHz~810MHz
-3dB frequency: 1GHz
IIP3: 27dBm at min gain, 1dBm at max gain
LO-RF and LO-IF isolation: under –75dB and about -49dB

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[1] Young-Jun Chong et al., "The design and implementation of TV for the digital terrestrial broadcasting," *Journal of KEES (Korea Electro-magnetic Engineering Society)*, vol. 11, no. 2, pp. 302-312, February 2000.

[2] A. Motamed et al., "CMOS exponential current-to-voltage converter", *Electronics Letters*, 5th June 1997, vol. 33, No. 13, pp. 998-1000.